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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,217	09/11/2003	John Michael Borkenhagen	ROC920030198US1	7696

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EXAMINER	
MERANT, GUERRIER	
ART UNIT	**PAPER NUMBER**
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,217	BORKENHAGEN ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20070510;20050131*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is the initial Office Action based on the application filed on September 11, 2003. Claims 1-16 are currently pending and have been considered below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by **Olsen (US 5,440,538)**.

As per claim 13: **Olsen** teaches a method for transmitting a block of data from a first electronic unit *(e.g. item 11, fig. 2)* to a second electronic unit *(e.g. item 13, fig. 2)* over a signaling bus, comprising the steps of:

identifying nonfaulty signaling conductors in the signaling bus *(e.g. col. 6, lines 65-68 & col. 5, lines 17-25)*; and transmitting the block of data using a transmission sequence from the first electronic unit to the second electronic unit, the transmission sequence utilizing all of the nonfaulty signaling conductors in the signaling bus; wherein the transmission sequence uses a minimum number of beats to complete the transmission of the block of data *(e.g. col. 6, lines 3-24)*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Olsen (US 5,440,538)** and further in view of **Izuno et al. (US 5, 717, 852).**

As per claims 1-2 & 6-7: **Olsen** substantially teaches a method for transmitting a "J" bit block of data from a first electronic unit *(e.g. item 11, fig. 2)* to a second electronic unit *(e.g. item 13, fig. 2)* over a signaling bus having "K" signaling conductors *(e.g. communication channel, item 10, fig. 2)*, where zero to "K-1" of the signaling conductors is faulty *(e.g. fig. 2 shows a single redundant spare link 19a (K = 1), which means k-1 are the number of defectives channels)*, the method comprising the steps of:

identifying faulty and nonfaulty signaling conductors in the signaling bus *(e.g. col. 6, lines 65-68 & col. 5, lines 17-25)*;

determining "F", the number of faulty signaling conductors in the signaling bus; determining "K-F", the number of nonfaulty signaling conductors in the signaling bus *(e.g. fig. 2 shows a single redundant spare link 19a (K = 1), which means k-1 are the number of defectives channels)*; and transmitting the "J" bit block of data over the "K-F" nonfaulty signaling conductors using "J/(K-F)" beats, plus an additional beat if a

remainder exists *(e.g. col. 6, lines 3-24).* But **Olsen** fails to explicitly teach setting a fault status of the signaling conductors in the first electronic unit and in the second electronic unit, using information found by the step of identifying faulty and nonfaulty signaling conductors in the signaling bus. However, **Izuno et al. (US 5,717,852)**, in analogous art, teaches a system/method for transmitting data between a bus-mater *(e.g. item 2B) and bus-slave (e.g. item 9, fig. 1)* via a plurality of buses comprising a bus status information keeping circuit (item 4, fig. 1) for storing information indicating about a faulty bus line (*e.g. col. 4, lines 23-34).*

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate the in the system/method of **Olsen** the bus status information taught in **Izuno et al.** in order to speed up data transfer and improve fault tolerance (e.g. col. 2, lines 15-20; **Izuno et al.**).

As per claims 8-11: **Olsen** substantially teaches an apparatus for transmitting a "J" bit block of data from a first electronic unit *(e.g. item 11, fig. 2)* to a second electronic unit *(e.g. item 13, fig. 2)* comprising:

a first block of data in the first electronic unit holding "J" bits for transmission; storage in the second electronic capable of holding a second block of data having "J" bits *(e.g. col. 4, lines 50-67)*; a signaling bus having "K" signaling conductors coupling the first electronic unit to the second electronic unit *(e.g. communication channel, item 10, fig. 2)*, the signaling bus having "F" faulty signaling conductors and "K-F" nonfaulty signaling conductors; determining "F" faulty signaling conductors and the "K-F"

nonfaulty signaling conductors on the signaling bus *(e.g. fig. 2 shows a single redundant spare link 19a (K = 1), which means k-1 are the number of defectives channels).* But **Olsen** fails to explicitly teach setting a fault status of the signaling conductors in the first electronic unit and in the second electronic unit, using information found by the step of identifying faulty and nonfaulty signaling conductors in the signaling bus, a diagnostic unit coupled to the first electronic unit and to the second electronic unit, and a driving sequencer in the first electronic unit that, respondent to the fault identification information, transmits the "J" bits of data using "J/(K-F)" beats, plus an additional beat if a remainder exists, using only the "K-F" nonfaulty conductors. However, **Izuno et al. (US 5,717,852)**, in analogous art, teaches a system/method for transmitting data between a bus-mater *(e.g. item 2B) and bus-slave (e.g. item 9, fig. 1)* via a plurality of buses comprising a bus status information keeping circuit (item 4, fig. 1) for storing information indicating about a faulty bus line (*e.g. col. 4, lines 23-34) and a* diagnostic unit coupled to the first electronic unit and to the second electronic unit *(e.g. items 6, 8, 11 & 13, fig. 1) to detect and reports faults in the bus system.*

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate the in the system/method of **Olsen** the bus status information taught in **Izuno et al.** in order to speed up data transfer and improve fault tolerance (e.g. col. 2, lines 15-20; **Izuno et al.**).

Claims 3 & 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Olsen (US 5,440,538)** and **Izuno et al. (US 5, 717, 852)** further in view of **Becker et al. (US 2004/0136319 A1).**

As per claims 3-5: **Olsen** and **Izuno et al.** fail to teach the step of storing the "F" bits further comprising the step of shifting at least one bit of the "F" bits into a first end of a shift register. However, **Becker et al.** teaches a method for managing a set of signal paths between a driver chip (e.g. item 100, fig. 1) and a receiver chip (e.g. item 102, fig. 1) comprising a testing system included a shift register unit (e.g. items 402-406, fig. 4) for storing data bits.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate in the receiver circuit of **Olsen** and **Izuno et al.** the shift register taught in **Becker et al.** in order *to handle defects or failures in signal paths between different chips (e.g. [0007]; Becker et al.).*

As per claim 12: **Olsen** and **Izuno et al.** fail to teach the second electronic unit further comprising a receiving sequencer coupled to the signaling bus and to the diagnostic unit, the receiving sequencer capable of storing "K-F" bits at a time into the second block of data, the "K-F" bits received from the "K-F" nonfaulty signaling conductors of the signaling bus, the receiving sequencer further capable of storing fewer than "K-F" bits if "J/(K-F)" has a remainder. However, **Becker et al.** teaches a method for managing a set of signal paths between a driver chip (e.g. item 100, fig. 1) and a

receiver chip (e.g. item 102, fig. 1) comprising a testing system included a shift register unit (e.g. items 402-406, fig. 4) for storing data bits.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate in the receiver circuit of **Olsen** and **Izuno et al.** the shift register taught in **Becker et al.** in order *to handle defects or failures in signal paths between different chips (e.g. [0007]; Becker et al.).*

Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Olsen (US 5,440,538)** and further in view of **Becker et al.**

As per claim 14: **Olsen** teach a method as in claim 13 above, but fails to teach the nonfaulty signaling conductors are identified during a power on sequence. However, **Becker et al.** teaches a method for managing a set of signal paths between a driver chip (e.g. item 100, fig. 1) and a receiver chip (e.g. item 102, fig. 1) wherein nonfaulty signaling conductors are identified during a power on sequence *(e.g. [0044])*. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate in the method of **Olsen** and **Izuno et al.** the testing method taught in **Becker et al.** in order *to handle defects or failures in signal paths between different chips (e.g. [0007]; Becker et al.).*

Claim 15: **Olsen and Becker et al.** teach a method as in claim 13 above, wherein the nonfaulty signaling conductors are identified by a wire test performed as a result of a

parity error, and error correcting code error, or a cyclical redundancy check error *(e.g. [0039] & [0044]; Becker* **et al**.*)*.

As per claim 16: **Olsen and Becker et al.** teach a method as in claim 13 above, further comprising the steps of: identifying a faulty signaling conductor in the signaling bus *(e.g. col. 6, lines 65-68 & col. 5, lines 17-25)*; and switching a driver coupled to the faulty signaling conductor to a high impedance state *(e.g. [0018]; Becker et al.)*.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner
Art Unit 2117

Guerrier Merant
05/31/07